AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF THE CLAIMS:

Claims 1-22 (Cancelled)

23. (Original) A semiconductor integrated circuit device comprising:

(a) three or more element forming regions formed on a surface of a semiconductor substrate and defined by an insulating film, said three or more element forming regions each extending in a first direction and being arranged in a second direction perpendicular to said first direction;

(b) a plurality of memory cells formed on each of said element forming regions, said memory cells each including:

(b_1) a first electrode constituted by a first conductive film formed through a first insulating film;

(b_2) a second electrode constituted by a second conductive film formed through a second insulating film on said first electrode, said second electrode extending in said second direction; and

(b_3) semiconductor regions formed on the element forming region on both sides of said second electrode,

wherein pseudo memory cells formed on an outermost element forming region out of said three or more element forming regions do not function as memory cells, and

wherein a semiconductor region of said pseudo memory cells is connected with ground potential.

24. (Original) A semiconductor integrated circuit device according to claim 23, wherein said second conductive film is in a floating state.

25. (Original) A semiconductor integrated circuit device according to claim 23, wherein said semiconductor region of said pseudo memory cells is in an OFF state.

26. (Original) A semiconductor integrated circuit device according to claim 23, wherein a connecting portion extending in said second direction is provided to connect end portions of said three or more element forming regions.

27. (Original) A semiconductor integrated circuit device according to claim 26, wherein said second conductive film is in a floating state.

28. (Original) A semiconductor integrated circuit device according to claim 26, wherein said semiconductor region of said pseudo memory cells is in an OFF state.

29. (Original) A semiconductor integrated circuit device according to claim 23, wherein said three or more element forming regions are arranged in said second direction perpendicular to said first direction, and

wherein a width in said second direction of an outermost element forming region out of said three or more element forming regions is larger than a width in said second direction of each of the other element forming regions.

30. (Original) A semiconductor integrated circuit device according to claim 29, wherein said second conductive film is in a floating state.

31. (Original) A semiconductor integrated circuit device according to claim 29, wherein said semiconductor region of said pseudo memory cells is in an OFF state.

32. (New) A method of manufacturing a semiconductor integrated circuit device comprising steps of:

(a) forming two or more element forming regions over a surface of a semiconductor substrate, said two or more element forming regions being defined by an insulating film and each extending in a first direction and being arranged in a second direction perpendicular to said first direction;

(b) forming a plurality of memory cells over main surfaces of said two or more element forming regions; and

(c) forming a conductive film over said semiconductor substrate so as to surround said plurality of memory cells,

wherein said element forming regions extend up to below said conductive film, which extends in said second direction.

33. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 32, wherein said step (b) includes:

(b_1) forming a first electrode through a first insulating film on one of said element forming regions;

(b_2) forming a second electrode through a second insulating film on said first electrode, said second electrode extending in said second direction; and

(b_3) forming semiconductor regions in the element forming region on both sides of said second electrode.

34. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 32,

wherein said memory cells are non-volatile memory cells.

35. (New) A method of manufacturing a semiconductor integrated circuit device comprising steps of:

(a) forming two or more element forming regions over a surface of a semiconductor substrate, said two or more element forming regions being defined by an insulating film and each extending in a first direction and being arranged in a second direction perpendicular to said first direction;

(b) forming a plurality of memory cells over main surfaces of said two or more element forming regions; and

(c) forming a conductive film over said surface of a semiconductor substrate, said conductive film extending in said second direction,

wherein said element forming regions extend up to below said conductive film.

36. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 35, wherein said step (b) includes:

(b_1) forming a first electrode through a first insulating film on one of said element forming regions;

(b_2) forming a second electrode through a second insulating film on said first electrode, said second electrode extending in said second direction; and

(b_3) forming semiconductor regions in the element forming region on both sides of said second electrode.

37. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 36,

wherein said memory cells are non-volatile memory cells.

38. (New) A method of manufacturing a semiconductor integrated circuit device comprising steps of:

(a) forming element isolation regions in a semiconductor substrate so as to provide two or more element forming regions over a surface of said semiconductor substrate;

(b) forming a plurality of memory cells over main surfaces of said two or more element forming regions; and

(c) forming a conductive film over said semiconductor substrate, said conductive film extending up to below said two or more element forming regions.

39. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 38, wherein said step (a) includes:

(a_1) forming grooves in said semiconductor substrate; and

(a_2) depositing an insulating film in said grooves.

40. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 38, wherein said step (b) includes:

(b_1) forming a first electrode through a first insulating film on one of said element forming regions;

(b_2) forming a second electrode through a second insulating film on said first electrode; and

(b_3) forming semiconductor regions in the element forming region on both sides of said second electrode.

41. (New) A method of manufacturing a semiconductor integrated circuit device according to claim 38,

wherein said memory cells are non-volatile memory cells.